A Framework for the Derivation of WCET Analyses for Multi-Core Processors

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Saarland University

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Context of Our Work

- Timing verification
  - Worst-case execution time (WCET) analysis
  - Scheduling theory / response time analysis

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- Scope of our work
  - WCET analysis for multi-core processors
  - Static analysis
  - Non-probabilistic
  - Not (yet) integrated with response time analysis

Motivation

Existing Work

WCET Analysis and Response Time Analysis for Multi-Core Processors

- [Kelter and Marwedel, 2014]
- [Chattopadhyay et al., 2012]
- [Schranzhofer et al., 2010]
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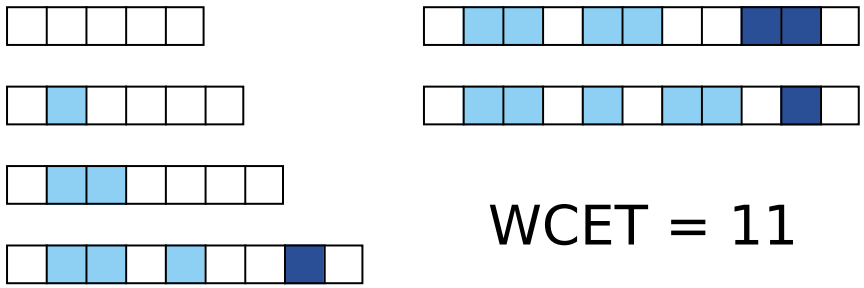
Motivating Example

All 6 Behaviors of a Simple Toy Program:



WCET = 11

□ = **non-interfered** execution

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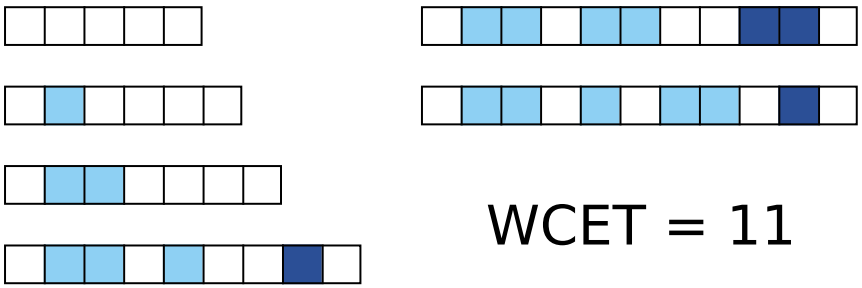

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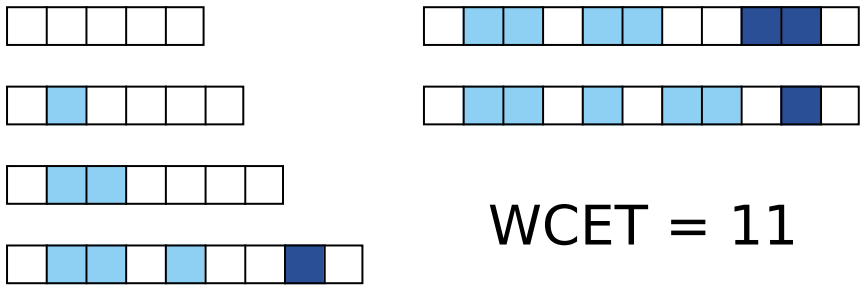

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□ = **non-interfered** execution

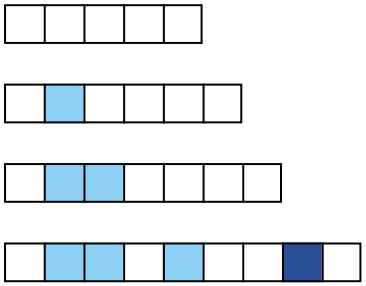
■ = **direct interference** effect

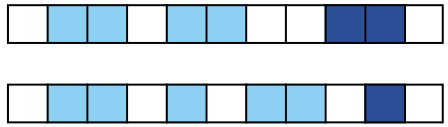
■ = **indirect interference** effect

- only as **consequence of** direct interference

Classical Compositional Timing Analysis

For our Example:





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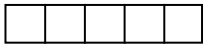
- Typical **compositional analysis**



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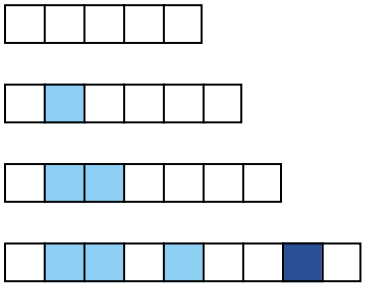

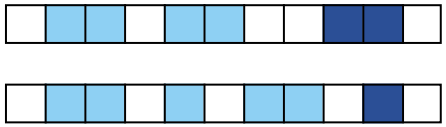

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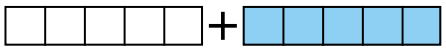 = 10 time units

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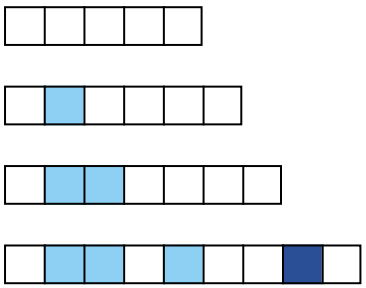

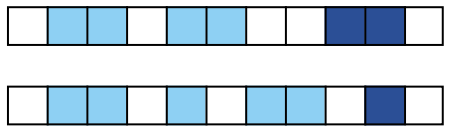

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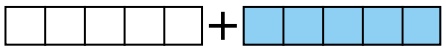

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Unsoundness

- Underestimates WCET

Increasing Penalty in Compositional Analysis

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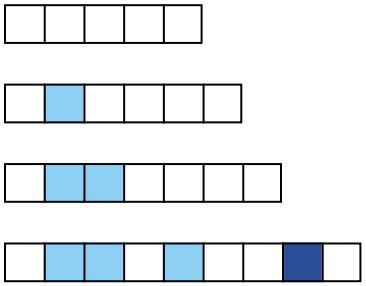

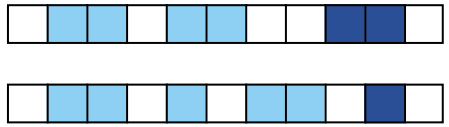

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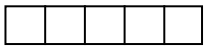

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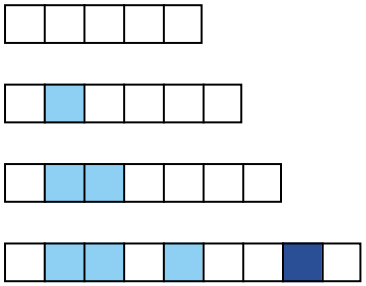

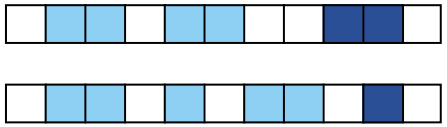

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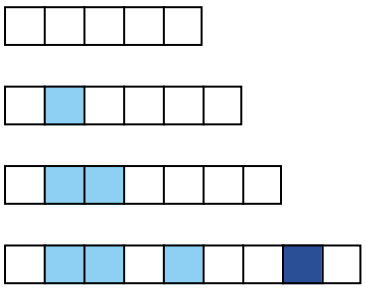

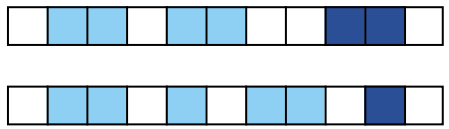

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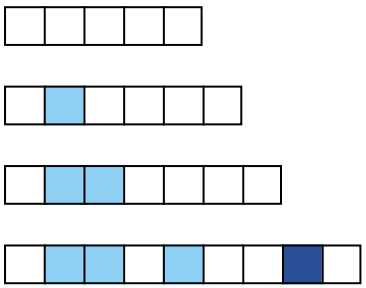

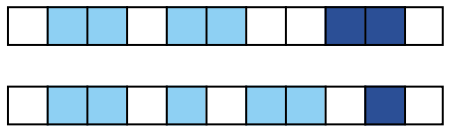

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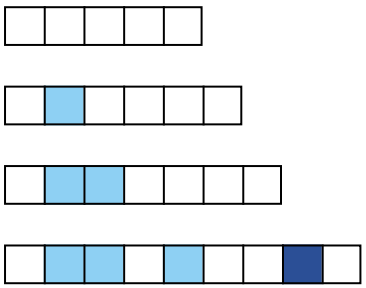

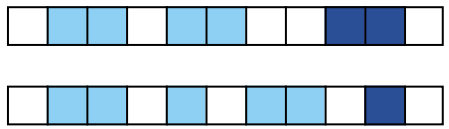

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Limitations

- Imprecision
- How to bound indirect effects per direct effect for a HW?
- Not possible for HW with domino effects!

A Novel Analysis by Us

"WCET Analysis for Multi-Core Processors with Shared Buses and Event-Driven Bus Arbitration" at RTNS 2015 [Jacobs et al., 2015]

- not compositional
  - explicitly models interference in core pipeline

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- not compositional
  - explicitly models interference in core pipeline
- sound & precise
- scalable
  - octa-core processors
  - out-of-order execution

Focus of This Talk

- Concepts
  - used during derivation of [Jacobs et al., 2015]

Our Paper

- embeds concepts in **formal framework**
- rigorous **soundness proofs**

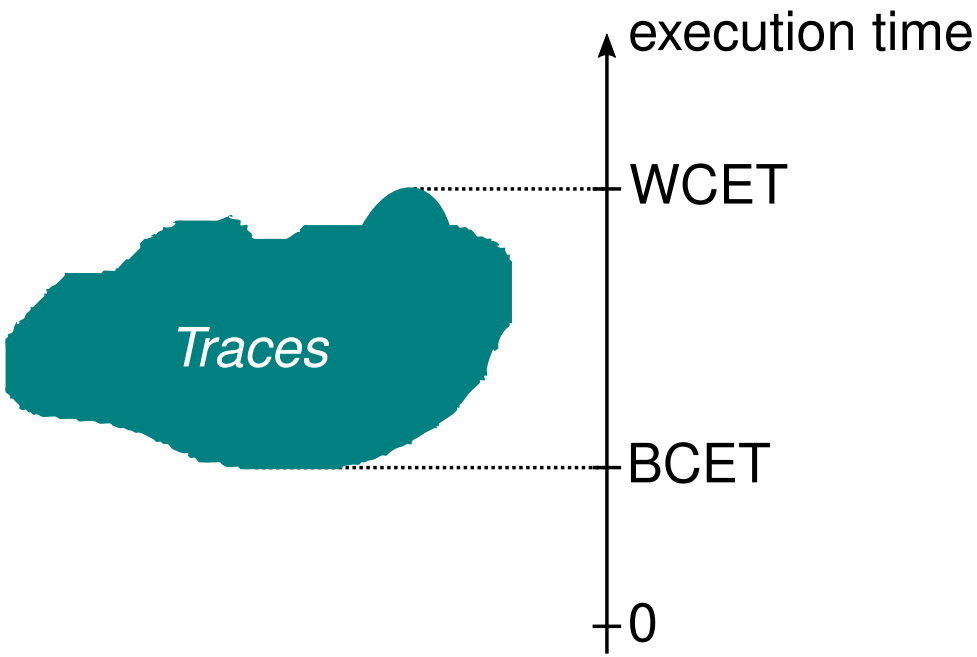
The Derivation of a WCET Analysis

Concrete-System Behavior

- Set *Traces* of system behaviors

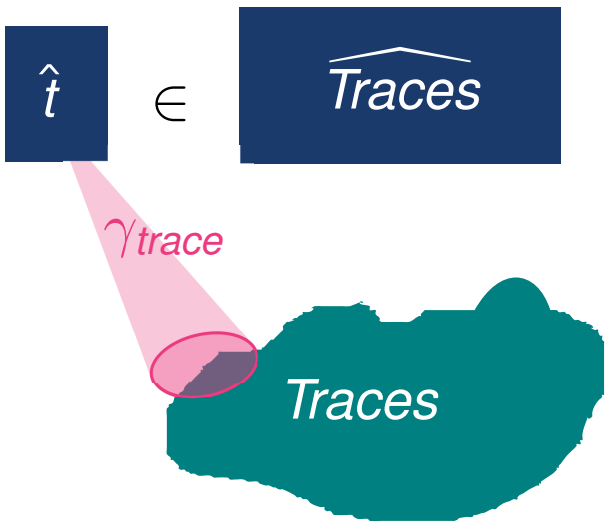
The Actual WCET

- Maximum execution time over all system behaviors



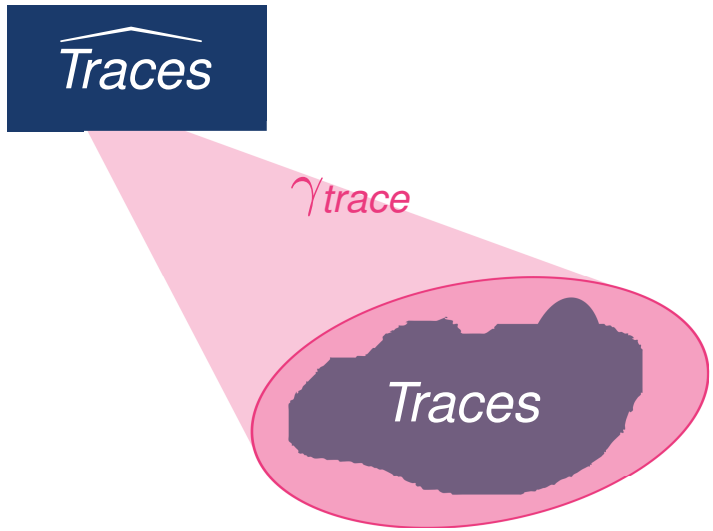
Approximation of System Behavior

- Set $\widehat{Traces}$ of **abstract traces**
- A $\hat{t} \in \widehat{Traces}$ describes (γ_{trace}):
  - system behaviors and/or
  - spurious behaviors



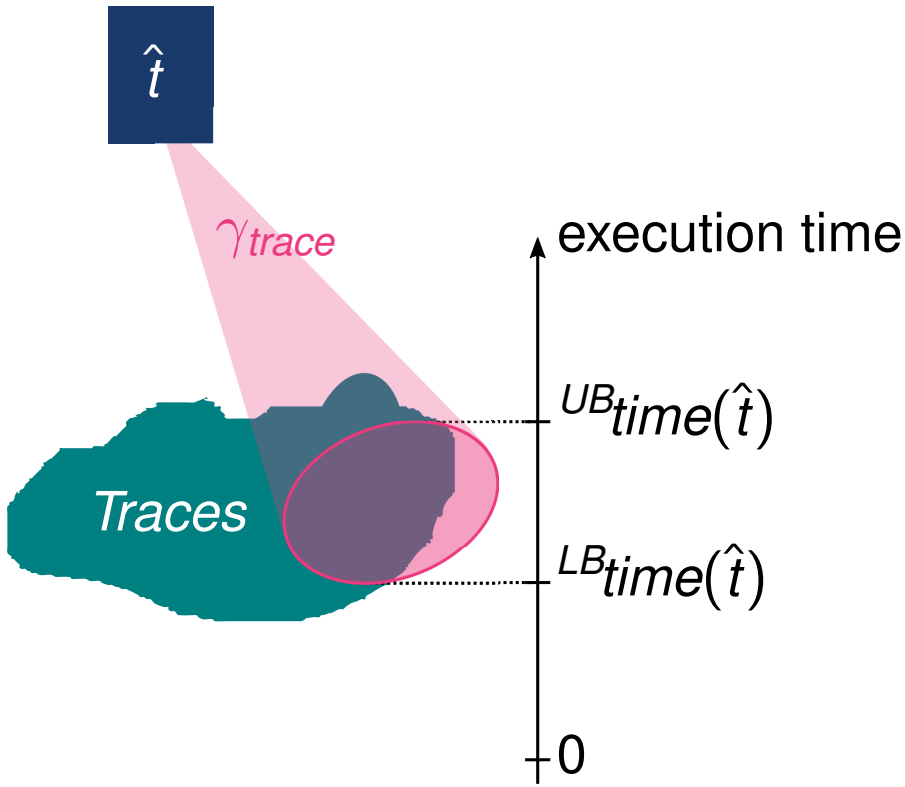
Soundness of an Approximation

- $\widehat{Traces}$ must overapproximate **all** system behaviors



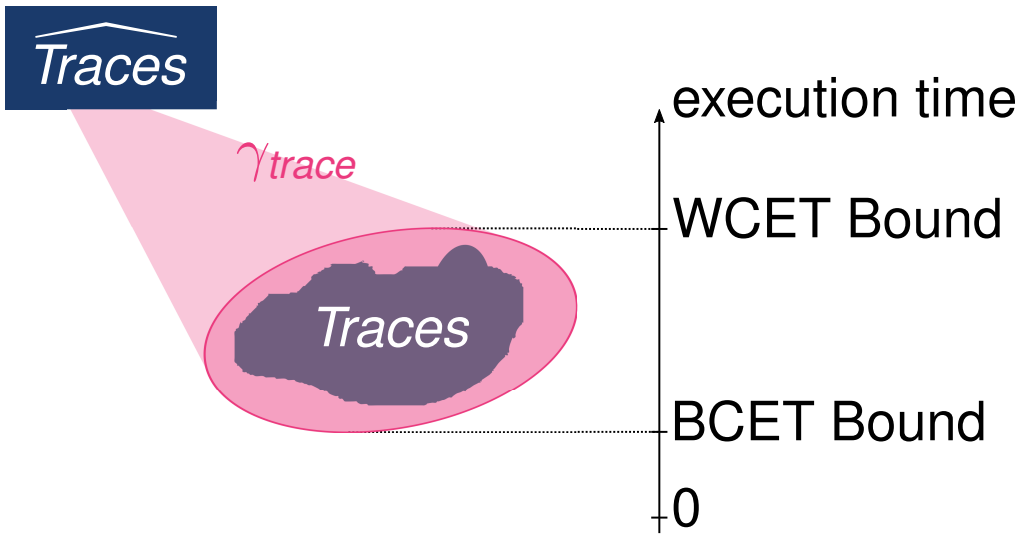
Time Bounds per Abstract Trace

- sound w.r.t. everything $\hat{t}$ describes



WCET Bound

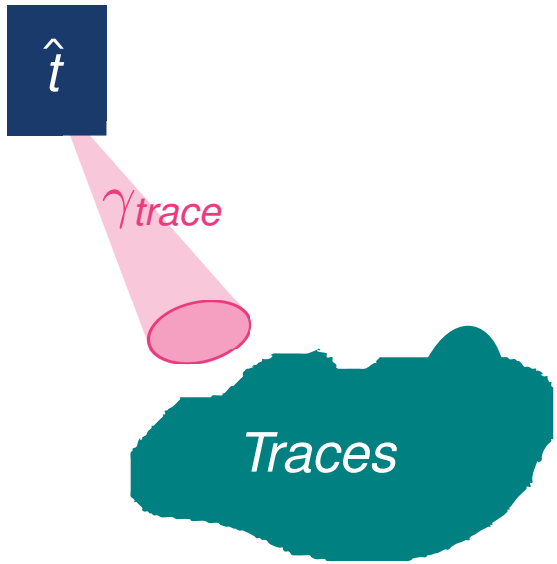
- $\max_{\hat{t} \in \widehat{Traces}} {}^{UB}time(\hat{t})$



Infeasible Abstract Traces

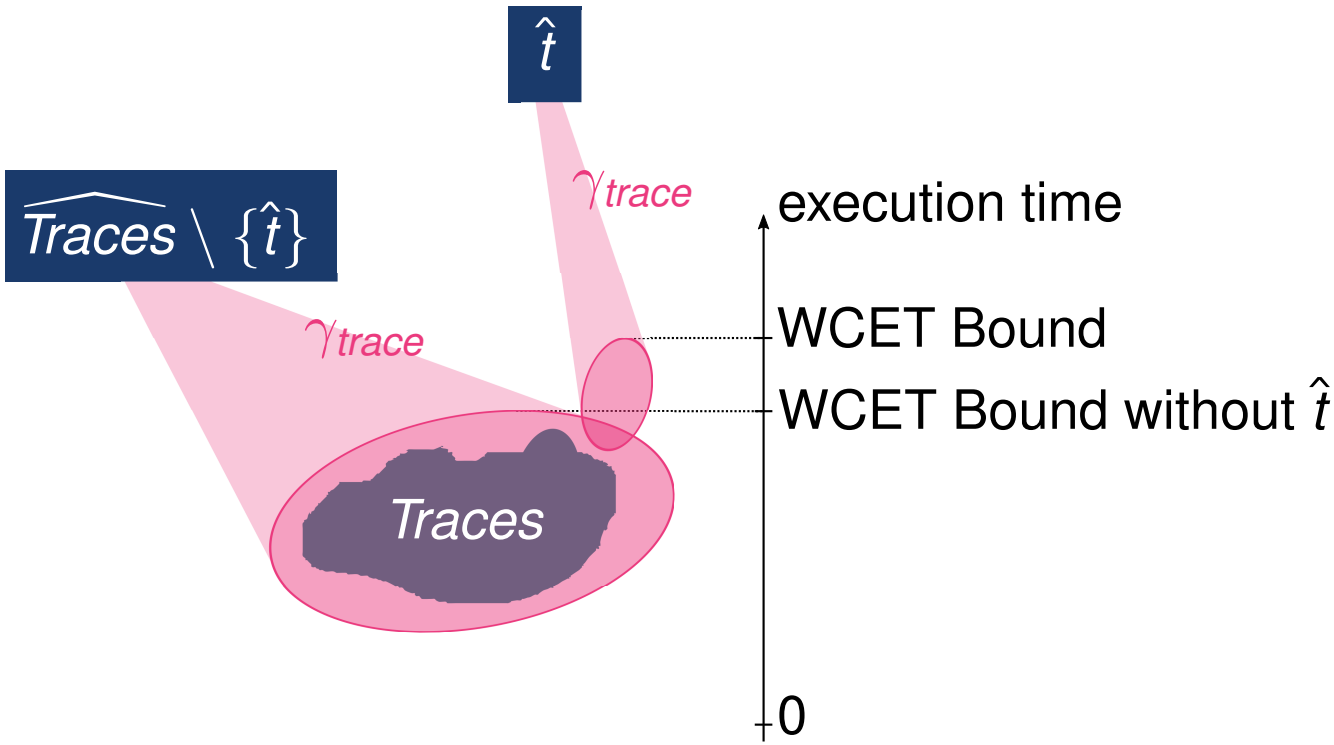
$$\widehat{Infeas} = \{\hat{t} \mid \hat{t} \in \widehat{Traces} \wedge \gamma_{trace}(\hat{t}) \cap Traces = \emptyset\}$$

- describe **only spurious** behavior



Impact of Infeasible Abstract Traces

- might **dominate** WCET bound



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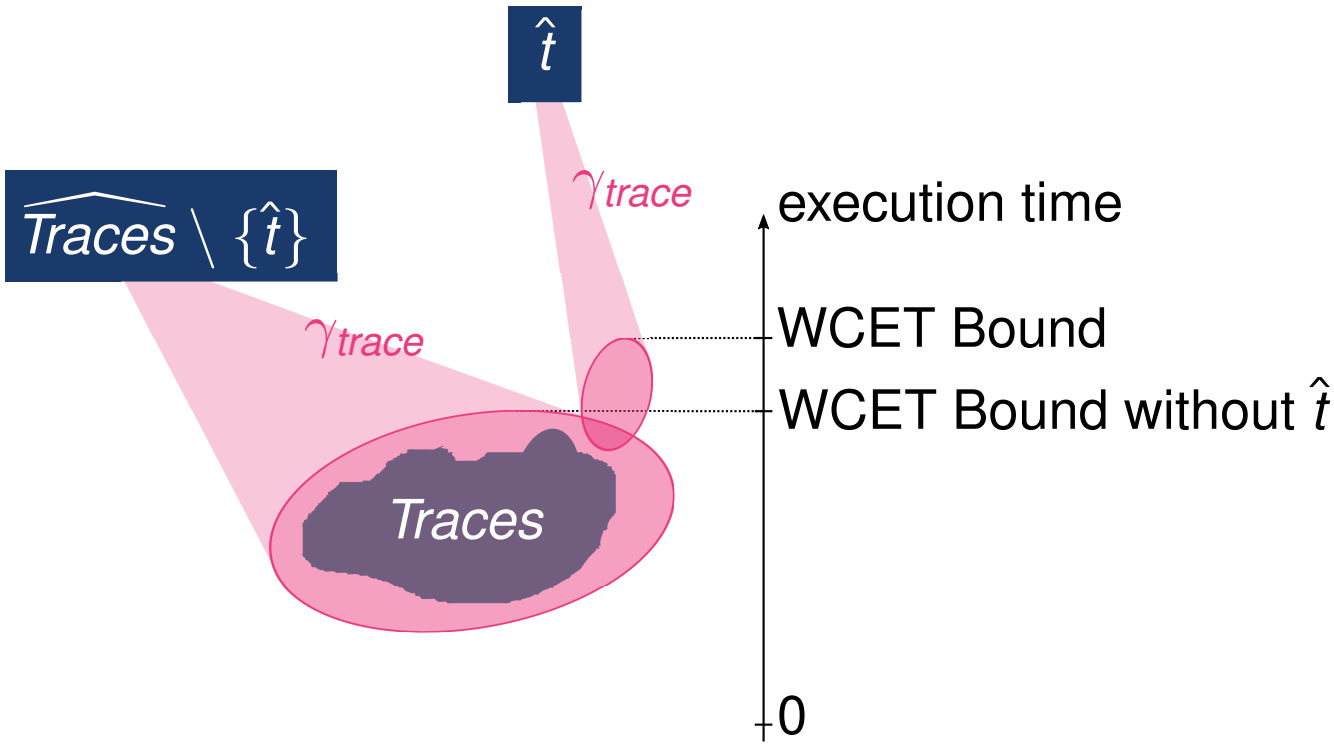

- Goal: **prune** them
  - How to detect them?

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- Property P
  - boolean predicate on execution behaviors

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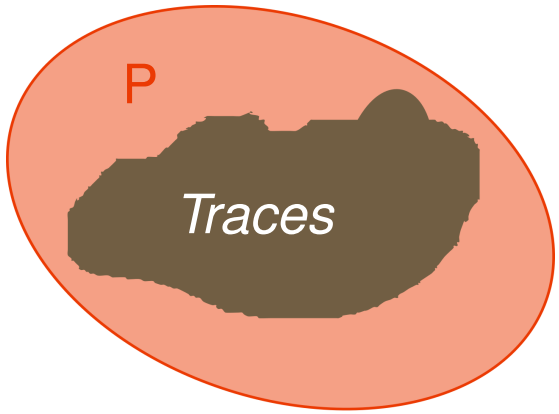
- Property *P*
  - boolean predicate on execution behaviors
- System property *P*
  - holds for each system behavior



Lifted System Property

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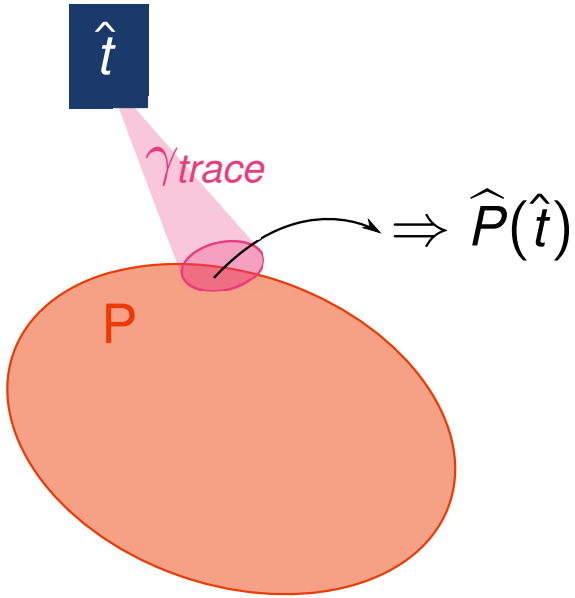
- Criterion:



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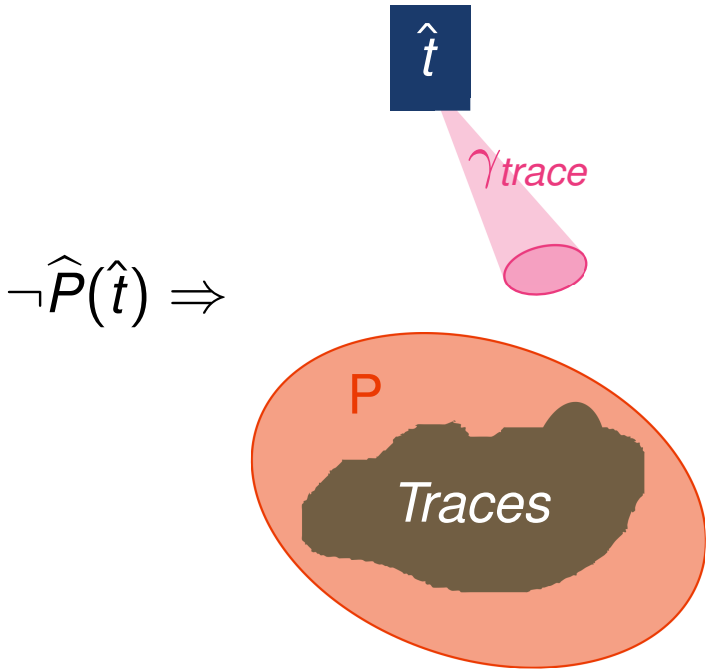

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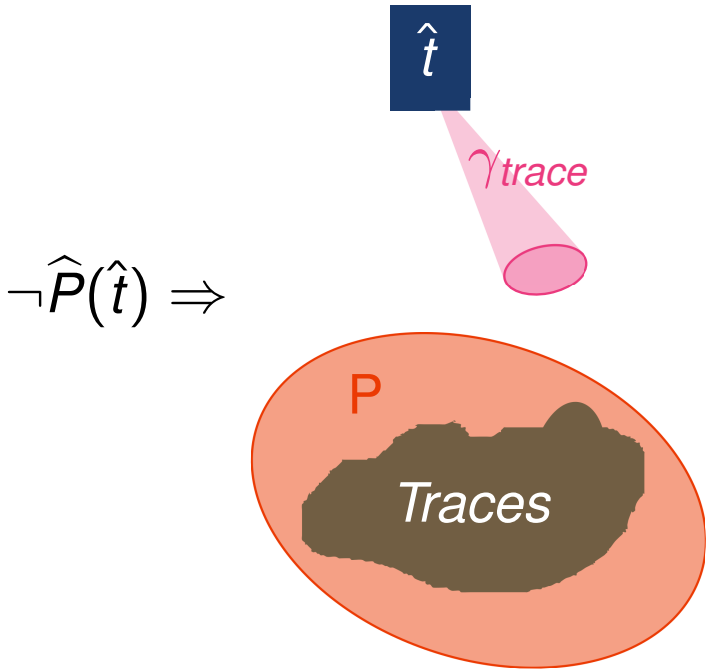

- not necessarily complete

Analysis Derivation Workflow

1. pessimistic **baseline approximation**

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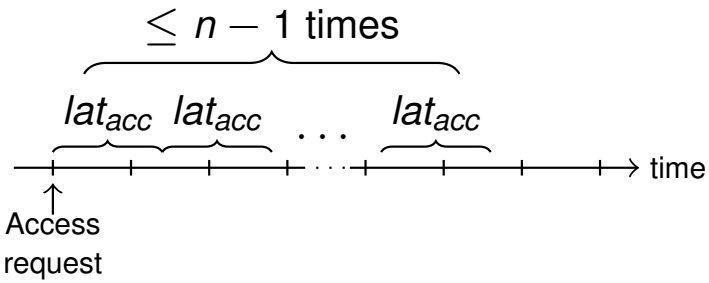
4. **implement** the analysis

Property Lifting Examples

Bounding Shared-Bus Delay

- round-robin bus arbitration
  - n-core processor



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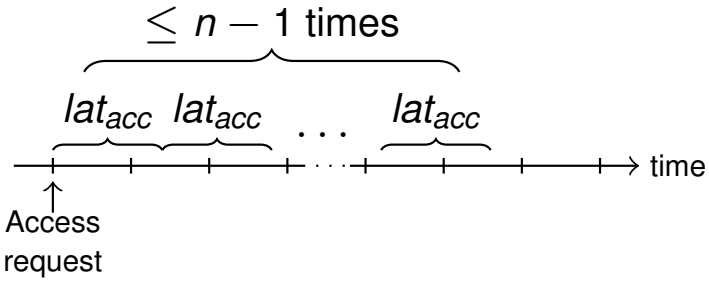

- $P(t) =$
  $\#blocked_{C_i}(t) \leq (n-1) \cdot lat_{acc} \cdot \#accesses_{C_i}(t)$

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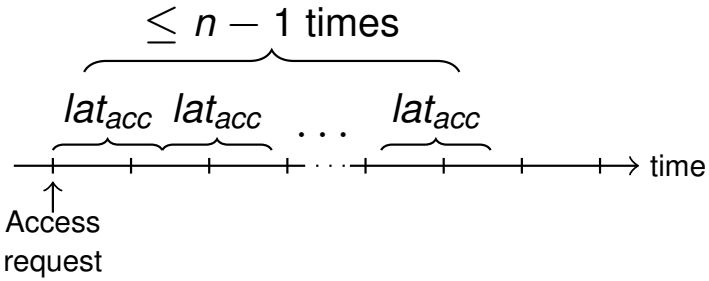

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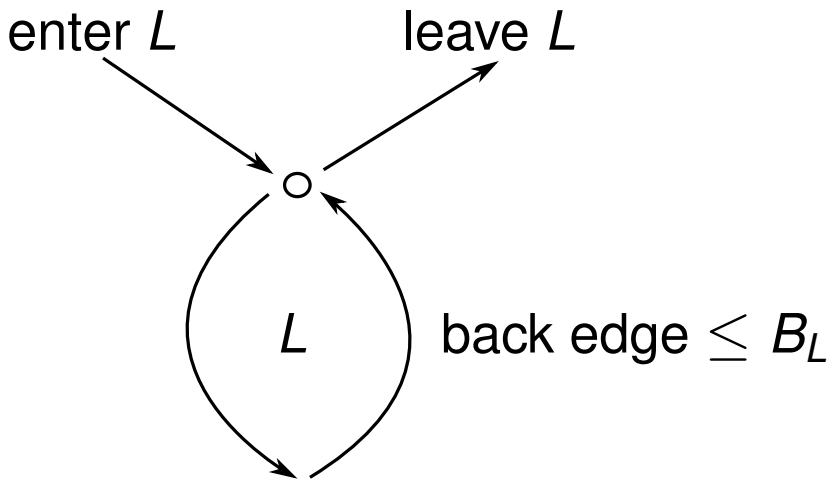
- $\widehat{P}(\hat{t}) =$
  ${}^{LB}\#blocked_{C_i}(\hat{t}) \leq (n-1) \cdot lat_{acc} \cdot {}^{UB}\#accesses_{C_i}(\hat{t})$

Bounding Loop Iterations

- loop bound B_L for loop L
  - back edge of L at most taken B_L times before L is left



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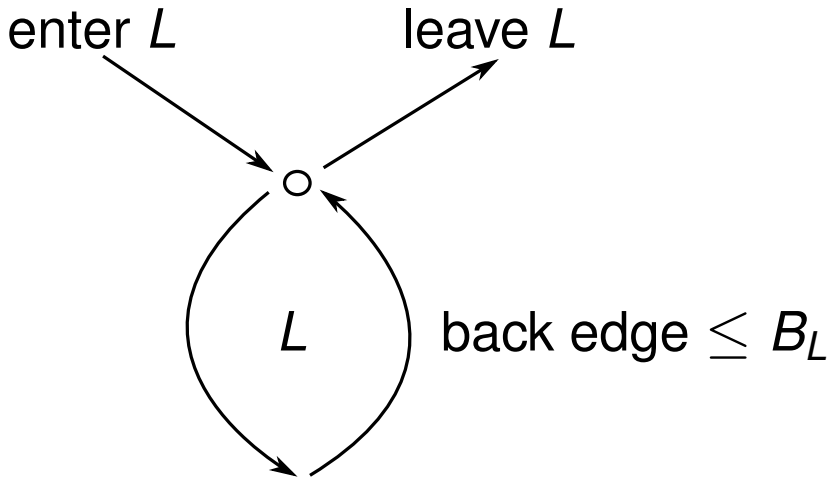

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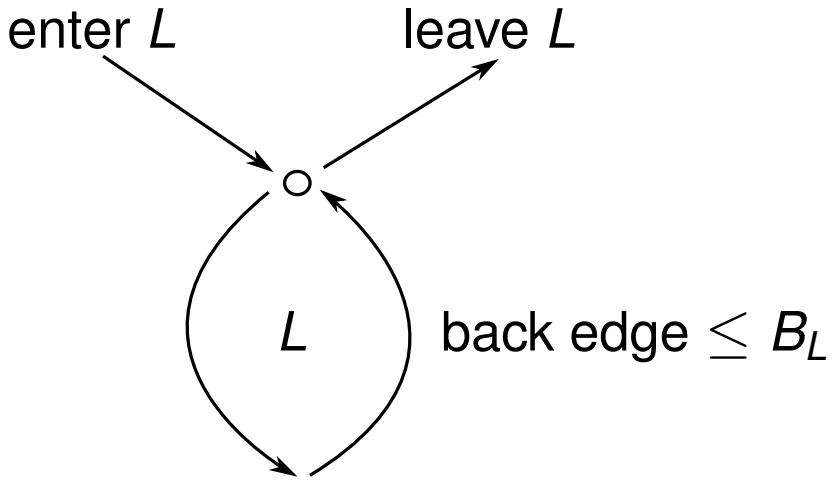
  $\#backEdge_L(t) \leq B_L \cdot \#entered_L(t)$

Bounding Loop Iterations



- loop bound B_L for loop L
  - back edge of L at most taken B_L times before L is left

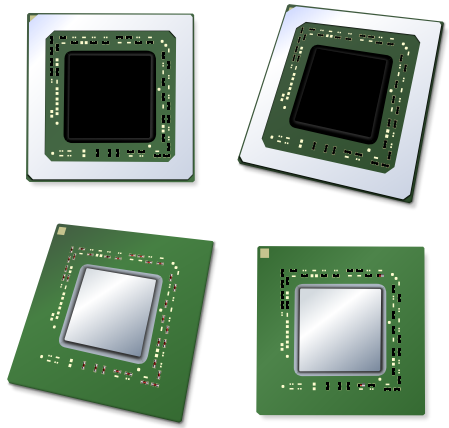
- $P(t) = \#backEdge_L(t) \leq B_L \cdot \#entered_L(t)$

- $\widehat{P}(\hat{t}) = {}^{LB}\#backEdge_L(\hat{t}) \leq B_L \cdot {}^{UB}\#entered_L(\hat{t})$

Experimental Evaluation

Experimental Setup

- Hardware platforms
  - ARM® instruction set
  - four processor-core configurations
  - round-robin shared bus
  - SRAM latency: 10 cycles
  - dual-, quad-, and octa-core



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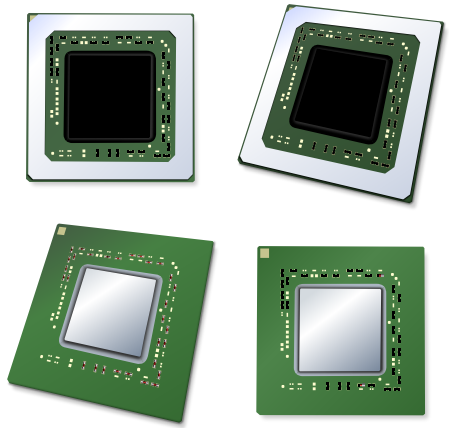

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  - 31 from Mälardalen suite
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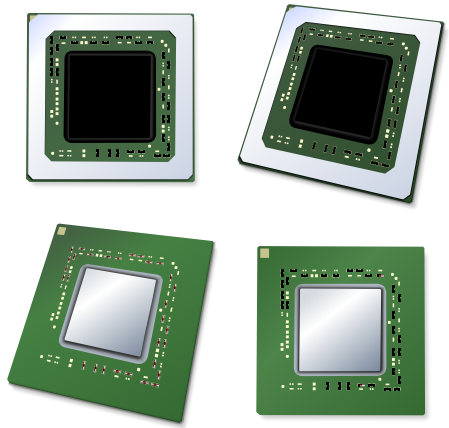

- Benchmarks
  - 31 from Mälardalen suite
  - 6 generated from SCADE models
- Analysis
  - **co-runner-insensitive** WCET bounds
  - per benchmark
  - per hardware configuration

Average Analysis-Runtime Increase

Compared to Compositional Analysis

- increasing **complexity** of processor cores

2-Core	in-order execution	out-of-order execution
local instruction scratchpad	3.3%	5.4%
local instruction cache	5.0%	15.9%

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- increasing **number** of processor cores
  - out-of-order execution, local instruction cache

2-Core	*4-Core*	*8-Core*
15.9%	15.2%	14.9%

What else is in the paper?

Co-Runner-Sensitive Analysis

- In this talk
  - co-runner-insensitive analysis

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- Goal
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Co-Runner-Sensitive Analysis

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  - e.g. under **work-conserving** bus arbitration
- Challenge
  - avoid enumerating all interleavings of access requests
- In our paper: **iterative overapproximation** algorithm
  - give up some precision
  - keep analysis runtime manageable

Summary

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- Formal framework
  - sound
  - modular
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Summary

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- Future work
  - shared caches
  - more processor-core features
  - integrate with response time analysis

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What Is an Abstract Trace?

- sequence of abstract states in **micro-architectural analysis**

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- ILP valuation in **implicit path enumeration**
  - lifted property implemented by constraints